GR 99 P 1493

Abstract

Circuit arrangement for processing an ATM cell header.

In contemporary transmission systems, information is transmitted in ATM cells which are routed (SDH) via a plurality of channels. In the prior art, for each channel there is provided one processing circuit in which a check information item representative of the cell header is generated, evaluated or corrected. The invention reduces the number of processing circuits by connecting upstream thereof FIFO memory devices which hold information relating to the cell header and supply it to the processing circuit, so that one processing circuit processes the cell header of ATM cells from a plurality of channels.

Figure 2